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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/707,844

11/08/2000

Hidetoshi Ishida

0819-448

9493

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04/05/2006

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EXAMINER

FARAHANI, DANA

ART UNIT

PAPER NUMBER

2891

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/707,844

Applicant(s)

ISHIDA ET AL.

Examiner

Dana Farahani

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 11-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 11-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue (US Patent 5,151,770).

Regarding claims 11 and 14, Inoue discloses in figure 1, a semiconductor device comprising:

A plurality of semiconductor elements, 24 and 26, formed on a semiconductor substrate 21; and

A plurality of through holes, which are provided between two adjacent ones of the plurality of semiconductor elements and pass from a surface through the backside of the semiconductor substrate 21, which is GaAs (see figure 5, and col. 9, lines 29-32. Note that the substrate should be 21 but has been indicated as substrate 1 in column 9).

Inoue does not expressly disclose a distance between two adjacent ones of the plurality of through holes (which is 100 microns. See col. 6, line 13) is smaller than a thickness of the semiconductor substrate. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to make the thickness of the substrate greater than 100 microns to have a solid support for the semiconductor device. See *In re Rose*, 105 USPQ.237 (CCPA 1955)

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for the proposition that a change in size is generally recognized as being within the level of ordinary skill in the art.

Regarding claim 12, the through holes are covered with a conductive material (see col. 8, lines 1-5).

Regarding claim 13, the conductive material is electrically connected to a ground wiring layer 52 (figs. 4 and 5) provided on the surface of the backside of the substrate (see col. 8, lines 1-5).

3. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue as applied to claims 11-14 above, and further in view of Nakamura et al., hereinafter Nakamura (US Patent 6,229,209).

Inoue renders obvious the limitations in the claims, as discussed above, except for a second group of through holes which are provided in electrodes of the plurality of semiconductor elements, pass from a surface through the backside of the substrate, and whose faces are covered with conductive material.

Nakamura discloses in figure 1, a second group of through holes 23 which are provided in electrodes of the semiconductor element 3, pass from a surface through the backside of the substrate 20, and whose faces are covered with conductive material 24 (see col. 6, lines 4-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to make connection to the semiconductor devices of the Inoue in the fashion of the Nakamura reference (which would lead to their connection to the backside ground wiring 52), commonly known as flip chip structure, in order to make contacts to the semiconductor components of the Inoue, and provide a ground voltage reference for those devices. Flip chip

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configurations and their advantages, such as occupying less space and making secure contacts are well known in the art.

Response to Arguments

4. Applicants' arguments filed 3/6/06 have been fully considered but they are not persuasive.

Applicants argue that the independent claim 11 recites that a distance between the two adjacent holes is smaller than the thickness of the substrate, and consider this as an important feature of the claimed invention. Applicants then argue that the motivation the examiner has provided (i.e. increasing the thickness of the substrate to have solid support for the semiconductor device) does not have any support (see the arguments filed on 3/6/06, page 6, first full paragraph).

In response to this argument, it is the position of the Office that such modification of the thickness of the substrate with the above mentioned motivation is generally known by persons with ordinary skill in the art. Also, Inoue discloses that the substrate must be large and strong enough to tolerate the manipulative assembly techniques (see col. 2, lines 5-9), thus confirming examiner's position that thickening the substrate [in accordance with the process which the device is made from] to make a solid support for the semiconductor device is within the general knowledge in the art. Also, see the case law cited above, which further confirms the examiner's motivation.

Applicants' argue that the Inoue reference clearly teaches that via holes are formed in the insulating films, and that the presence of the via holes therein are more important than forming

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them in the substrate, and therefore, the teachings of the reference are contrary to that of the applicants (see pages 5 and 6 of the remarks). The fact that via holes are formed in the insulating films above the substrate has nothing to with forming via holes in the substrate, which the Inoue reference clearly discloses, as discussed in the above rejections.

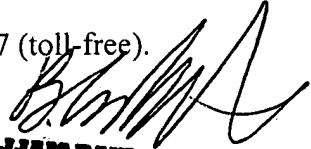
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571)272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Farahani


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